

A cross-sectional view of a semiconductor device. A substrate 2 is shown at the bottom. A layer 3 is formed on the substrate. A central gate structure 4 is formed on layer 3. The gate structure 4 has a central region 320 and side regions 325. The height of the gate structure 4 is denoted by 'h'. A layer 5 is formed on the gate structure 4. A layer 6 is formed on layer 5. A layer 31 is formed on the substrate 2. The width of the central region 320 is denoted by 'd'. The width of the side regions 325 is denoted by 'c'. The total width of the gate structure 4 is denoted by 'p'. The device is labeled 1.